

REMARKS

Applicant respectfully requests reconsideration of the above identified application. As of the Examiner's Amendment and Notice of Allowance mailed on February 12, 2007, Claims 16, 18, 21-24 and 39-44 were pending. Claims 16, 18, 21-22, 39-41 and 43-44 are rejected. Claims 23 and 24 are allowed. Claim 42 is objected to.

The Office Action mailed on May 31, 2007, rejects claim 16 under 35 USC 102(e) as allegedly being anticipated by US Patent 5,996,066 (Yung). Applicant respectfully disagrees.

Analysis of the instant claims should not occur in a vacuum but should correlate each claim element with corresponding structures, materials or acts set forth in the specification.

The Federal Circuit makes it clear that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention. "The person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Phillips v. AWH Corp.*, 415 F.3d at 1313.

Claim 16 sets forth:

16. (Previously Presented) A processor comprising:
a decode unit to decode a plurality of packed data instructions including a packed sum of absolute differences (PSAD) instruction having a first format to identify a first set of packed data, and a packed multiply-add (PMAD) instruction having a second format to identify a second set of packed data, said decode unit to initiate a first set of operations on the first set of packed data responsive to decoding the PSAD instruction and to initiate a second set of operations on the second set of packed data responsive to decoding the PMAD instruction; and
an execution unit to perform a first operation of the first set of operations initiated by the decode unit and to perform a second operation of the second set of operations initiated by the decode unit.

The Examiner indicates that the "pixel distance" of Yung (col. 5 lines 25-27) would be interpreted as the packed sum of absolute differences (PSAD) instruction and that the "single instruction [that] does both a multiply of two partitioned values, and an add with a separate, third value, with a masking capability," (col. 2 lines 10-14) would be interpreted as the packed multiply-add (PMAD) instruction.

Applicant respectfully submits that one skilled in the art would distinguish at least between the multiply-accumulate with masking instruction of Yung and the claimed PMAD instruction. In fact Yung distinguishes between them (e.g. col. 6, line 51-53) saying that, “The result of the multiplication is added in an adder/subtractor 96 with a value from a register 98 (as opposed to adding together partitioned fields of the multiply result as done in the Intel MMX instruction).” (i.e. PMAD).

Applicant further submits that Yung does not disclose enough to anticipate the PSAD instruction, but if one skilled in the art is presumed to understand the vis_pdist instruction of Sun Microsystems, Inc., then one skilled in the art would also distinguish between it and the claimed PSAD instruction.

Further, what Yung does disclose about the pixel distance instruction (e.g. Fig. 5, 56) is enough for one skilled in the art to determine that execution unit 28 (in Fig. 1; or 38 in Fig. 2; or execution unit 58 in Fig. 5) is not the same as execution unit 26 (in Fig. 1 or in Fig. 2; or execution unit 56 in Fig. 5) and does not perform both the first operation of the first set of operations initiated responsive to decoding the PSAD instruction and the second operation of the second set of operations initiated responsive to decoding the PMAD instruction, as claimed.

Therefore, Applicant respectfully submits that the Examiner has failed to establish a *prima facie* case of anticipation with regard to the claimed subject matter.

The Office Action further rejects claim 16 and also rejects claim 18 under 35 USC 103 as allegedly being unpatentable over Yung in view of US Patent 5,734,874 (Van Hook) and rejects claims 21-22 under 35 USC 103 as allegedly being unpatentable over Yung in view of Van Hook and further in view of US Patent 5,721,697 (Lee). Applicant respectfully disagrees.

Applicant respectfully submits the additional disclosure of PDIST (e.g. with regard to Fig. 9a) supports the assertion that one skilled in the art would distinguish between it and the claimed PSAD instruction.

Further, Figs. 2 and 5 of Yung and of Van Hook appear identical and to one skilled in the art, would establish that a single execution unit would not be expected to perform both the first operation of the first set of operations initiated responsive to decoding the PSAD instruction and the second operation of the second set of operations initiated responsive to decoding the PMAD instruction, as set forth in claim 16.

The disclosure of Lee is insufficient to remedy the problems of Yung and of Van Hook. Therefore, Applicant respectfully submits that the Examiner has failed to establish a *prima facie* case of obviousness with regard to the claimed subject matter.

The Office Action rejects claims 39-41 under 35 USC 102(e) as allegedly being anticipated by Van Hook. Applicant respectfully disagrees.

Claim 39 sets forth:

39. (Previously Presented) A processor comprising:
decode logic to decode a packed sum of absolute differences (PSAD) instruction having a first format to identify a first set of packed data, said decode logic to initiate a first set of operations on the first set of packed data responsive to decoding the PSAD instruction, the first set of operations comprising:
a packed subtract and write carry (PSUBWC) operation;
a packed absolute value and read carry (PABSRC) operation; and
a packed add horizontal (PADDH) operation.; and
execution logic to perform the first set of operations initiated by the decode logic.

Again, Applicant submits that analysis of the instant claim should not occur in a vacuum but should correlate each claim element with corresponding structures, materials or acts set forth in the specification. The meaning of a claim term must be the meaning that the term would have to a person of ordinary skill in the art not only in the context of the particular claim in which the term appears, but in the context of the entire patent, including the specification.

Van Hook discloses (col. 5, lines 11-17) that “At each dispatch, the PDU 46 may dispatch either a pixel distance computation instruction, a graphics data partitioned multiplication instruction, a graphics data packing instruction, or a graphics data compare instruction to the second partitioned execution path 34. The pixel distance computation circuit 56 executes the pixel distance computation instruction.”

Thus one skilled in the art would determine that the PDU 46 does not anticipate the claimed decode logic to initiate the three claimed operations responsive to decoding the PSAD instruction, but simply dispatches the PDIST instruction of Van Hook.

Two prior techniques for computing an absolute differences found in the design of floating point mantissa arithmetic are: (1) compare two numbers and reorder to subtract the smaller from the larger, or (2) subtract the two numbers in both directions and select the positive result. Applicant respectfully submits that in the context of the entire patent including the specification, one skilled in the art would distinguish between

the two techniques listed above and the claimed packed subtract and write carry (PSUBWC) operation and the packed absolute value and read carry (PABSRC) operation set forth by the present application.

Van Hook discloses (col. 10, line 65 through col. 11, line 9) that, “As shown in FIG. 9b, in this embodiment, the pixel distance computation circuit 56 comprises eight pairs of 8 bit subtractors 57a-57h. Additionally, the pixel distance computation circuit 56 further comprises three 4:2 carry save adders 61a-61c, a 3:2 carry save adder 62, two registers 63a-63b, and a 11-bit carry propagate adder 65, coupled to each other as shown. The eight pairs of 8 bit subtractors 57a-57h, the three 4:2 carry save adders 61a-61c, the 3:2 carry save adder 62, the two registers 63a-63b, and the 11-bit carry propagate adder 65, cooperate to compute the absolute differences between eight pairs of 8-bit values, and aggregate the absolute differences into a 64-bit sum.”

Thus from Fig. 9b of Van Hook and the above disclosure, one of skill in the art may conclude that Van Hook performs the second known technique (2) rather than the claimed PSUBWC operation and the PABSRC operations.

The Examiner claims that subtractors 57a-57h write carries, and that multiplexers 59a-59h read carries, but Applicant respectfully finds no storage elements, to which carries may be written, or from which carries may be read, consistent with what would be understood from the claimed PSUBWC operation and the PABSRC operations by one skilled in the art in the context of the entire patent including the specification.

Moreover Van Hook uses the word “carry” six times in the above paragraph (col. 10, line 65 through col. 11, line 9) but not once with regard to subtractors 57a-57h or multiplexers 59a-59h or any kind of storage of carries to be written or read between them.

Therefore, Applicant respectfully submits that the Examiner has failed to establish a *prima facie* case of anticipation with regard to the claimed subject matter.

The Office Action rejects claims 43-44 under 35 USC 103 as allegedly being unpatentable over Van Hook in view of Lee. Applicant respectfully disagrees.

The disclosure of Lee is insufficient to remedy the problems of Van Hook with regard to claim 39. Moreover, Van Hook discloses (col. 5, lines 16-19) that the pixel distance computation circuit 56 executes the pixel distance computation instruction, but

partitioned multiplier 58 executes the graphics data partitioned multiplication instructions.

Thus without a suggestion to modify Van Hook, it must be assumed that the combination results from impermissible hindsight using Applicant's own disclosure. Therefore, Applicant respectfully submits that the Examiner has failed to establish a *prima facie* case of obviousness with regard to the claimed subject matter.

CONCLUSION

Applicant respectfully submits the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Lawrence Mennemeier at (408) 765-2194.

Authorization is hereby given to charge our Deposit Account No. 50-0221 for any charges that may be due.

Respectfully submitted,

Date: November 28, 2007

/s/Lawrence M. Mennemeier/

Lawrence M. Mennemeier
Reg. No. 51,003

INTEL CORPORATION
c/o INTELLEVATE LLP
P.O. Box 52050
Minneapolis, MN 55402
(408) 765-2194